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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,982	01/29/2002	Danielle A. Thomas	98-C-152C1 (STMI01-00043)	8483
30425	7590	04/27/2005	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			TRINH, HOA B	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/059,982

Applicant(s)

THOMAS, DANIELLE A.

Examiner

Vikki H. Trinh

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02/28/05.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 and 14-27 is/are pending in the application.
- 4a) Of the above claim(s) 9, 22 and 23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 14-21 and 24-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-8, 14-21, 24-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In the original specification and figures 1C and 3, capacitive electrodes 136 (fig. 1C) and 302 (fig. 3) are directly connected with another conductive layer 132 (fig. 1C) and 312 (fig. 3), respectively, thereby preventing the capacitive electrode from forming a capacitor because the current from the first conductive layer would flush through the capacitive electrode. This means a capacitor is not formed. Therefore, claims 1-8, 14-21, 24-27 fail to comply with enablement requirement.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Art Unit: 2814

2. Claims 1-8, 14-21, 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Rhodes (6,852,591)

Rhodes discloses, as to claims 1, 6, an integrated circuit structure having a capacitive electrode 160 (fig. 14) proximate to a sensing surface 116 (fig. 14) on which an object is placed, the capacitive electrode 160 (fig. 14) forms a capacitor 162 (fig. 14) with the object; a dielectric 158 (fig. 14) underlying the electrode 160 (fig. 14) for forming a capacitor 162 (fig. 14); and an active region 108 (fig. 14, col. 8, lines 62-65) underlying the dielectric 158 (fig. 14) wherein the electrode 160 (fig. 14) and all conductive regions 160, 156, and/or 108 (fig. 14) are formed of a conductive material, tungsten (col.9, lines 65-67 and col. 10, line 24).

As to claim 2, the electrode 160 and the conductive region 156 are formed of a conductive material that is as great as a hardness of the dielectric 158 (fig. 14).

As to claims 3, 16, 25, a passivation layer 164 (fig. 14) over the electrode 160 (fig. 14), the passivation layer 164 (fig. 14) forming the sensing surface, wherein the electrode 160 (fig. 14) and the conductive regions 156 are formed of material that is as great as a hardness of the passivation layer (col. 10, lines 31-32).

As to claims 5, 18-19, the structure includes a tungsten via 150 (col. 9, lines 50-55) which includes the interconnect 150 (fig. 14).

As to claims 7, 20, the structure includes a tungsten contact 150 (fig. 14).

As to claims 8, 21, the active region 108 (col. 8, lines 62-65, fig. 14) is a gate electrode.

As to claims 14-15, 17, Rhodes also teaches a method of forming a scratch resistant integrated circuit having the steps of forming an active region 108 (fig. 14); forming a dielectric 158 or 106 (fig. 14) overlying the active region; and forming an electrode 160 (fig. 14)

Art Unit: 2814

overlying the dielectric 158 (silicon dioxide) proximate to a sensing surface 116; the electrode 160 (fig. 14) and the conductive region 156 (fig. 14) are formed of tungsten (col.9, lines 65-67 and col. 10, line 24) which is harder than aluminum or silicon dioxide layer, as applicant's claim

As to claims 24, 26, a method of forming a scratch resistant integrated circuit structure having a plurality of active regions 108 (fig. 14) , forming a dielectric 158 or 106 (fig. 14) over the plurality active regions; and forming an array of capacitive electrodes 160 (fig. 14) made of tungsten (col.9, lines 65-67 and col. 10, line 24) overlying the dielectric proximate to a sensing surface (fig. 14) on which an object is selectively placed, the capacitive electrodes 160 (fig. 14) each forming a capacitor 162 (fig. 14) with the object when the object is placed on the sensing surface and wherein the capacitive electrodes 160 (fig. 160) are each formed of a conductive material having a hardness at least as great as a hardness of the dielectric. The examiner note that the dielectric layer is made of silicon dioxide and the conductive material is made of tungsten and/or its alloys. Also note that Rhodes discloses more than one capacitor making it an array.

As to claim 27, the method includes forming each metallization region 156 (fig. 14) (tungsten) between the array of electrodes 160 (fig. 14) and the plurality of the active regions 108 of a conductive material having the hardness at least as great as the hardness of the dielectric 158 (col.9, lines 65-67 and col. 10, line 24).

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-8, 14-21, 24-27 have been considered but are moot in view of the new ground(s) of rejection.

### Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh  
Patent Examiner  
5/22/05



HOWARD WEISS  
PRIMARY EXAMINER